THE CLAIMS

What is claimed is:

1. A method comprising:

serializing an N-bit data to generate a digital voltage sequence;

converting the digital voltage sequence to a first current signal having an adjustable bias mode and an adjustable modulation mode;

driving a first laser using said first current signal to generate a first optical signal transmission;

converting a second optical signal reception into a first single-ended voltage signal;

complimentary coupling said first single-ended voltage signal with a second single-ended voltage signal to generated a differential data voltage signal; and

resistively coupling said first and second single-ended voltage signals to attenuate a common signal noise.

2. The method of Claim 1 further comprising:

generating a digital clock signal;

using the digital clock signal to generate the digital voltage sequence from the N-bit data;

converting the digital clock signal to a second current signal having an adjustable bias mode and an adjustable modulation mode;

driving a second laser using said second current signal to generate a third optical signal transmission.

3. The method of Claim 2 further comprising:

adjusting said modulation mode of the second current signal.

4. The method of Claim 3 further comprising:

adjusting said bias mode of the second current signal.

5. The method of Claim 2 further comprising:

converting the third optical signal reception into a third single-ended voltage signal;

complimentary coupling said third single-ended voltage signal with a fourth single-ended voltage signal to generate a differential clock signal; and

recovering the digital clock signal from the differential clock signal.

6. The method of Claim 5 further comprising:

generating a plurality of clock phases from the differential clock signal in a delay locked loop; and

interpolating the plurality of clock phases to align a clock edge of the digital clock signal with respect to the differential data voltage signal.

7. The method of Claim 1 further comprising:

adjusting said modulation mode of the first current signal by setting one or more modulation control inputs.

8. The method of Claim 1 further comprising:

adjusting said bias mode of the first current signal by setting one or more bias control inputs.

9. An optical transmitter comprising:

a phase locked loop circuit to generate a clock signal;

a serializer circuit to receive the clock signal and to convert an N-bit data to a digital voltage sequence;

a laser driver having a bias control and a modulation control, said laser driver to receive the digital voltage sequence and to generate a current signal having a bias mode adjustable by said bias control and a modulation mode adjustable by said modulation control; and

a laser to generate an optical signal responsive to the current signal of the laser driver.

10. The optical transmitter of Claim 9 further comprising:

a buffered level shifter circuit tunable through k+1 control signals to shift an input of the laser driver to a controlled voltage level at a controlled rate and with adjustable impedance responsive to a transition of said digital voltage sequence.

11. The optical transmitter of Claim 10, said laser driver further comprising:

a CMOS modulation circuit having a pMOSFET, a first nMOSFET and a second nMOSFET, the CMOS modulation circuit to cause the current signal of the modulation

mode to flow from a laser power source through the first nMOSFET and second nMOSFET responsive to the input of the laser driver being shifted to a first voltage level, and to causes the current signal of the bias mode to flow from the laser power source through the bias control when another current flows from a second power source through the pMOSFET responsive to the input of the laser driver being shifted to a second voltage level.

12. The optical transmitter of Claim 11 wherein an input gate of the third nMOSFET is coupled with the second power source to reduce an overshoot of the current signal.

13. The optical transmitter of Claim 10 further comprising:

a plurality of capacitors coupled with the bias control to reduce a frequency dependent component of impedance.

14. The optical transmitter of Claim 9 wherein the laser driver is a CMOS circuit.

15. The optical transmitter of Claim 14 wherein the laser is a VCSEL diode.

16. The optical transmitter of Claim 9 wherein adjusting the modulation mode of the current signal is accomplished by setting one or more inputs of the modulation control.

17. The optical transmitter of Claim 9 wherein adjusting the bias mode of the current signal is accomplished by setting one or more inputs of the bias control.

18. An optical receiver comprising:

a first photo-detector to receive a first optical signal and to generate a first current signal;

a first transimpedance amplifier circuit to convert the first current signal to a first differential voltage signal;

a clock recovery circuit having a phase interpolator to generate an aligned clock signal for said first differential voltage signal;

a sampler circuit to receive the aligned clock signal and to receive the differential voltage signal and to generate a digital voltage sequence; and

a deserializer circuit to receive the digital voltage sequence and to generate an N-bit data.

19. The optical receiver of Claim 18 wherein said first transimpedance amplifier circuit complimentary couples a first single-ended voltage signal corresponding to the first current signal with a second single-ended voltage signal to generated said first differential voltage signal, and resistively couples said first and second single-ended voltage signals to attenuate a common signal noise.

20. The optical receiver of Claim 19, said first transimpedance further comprising:

a differential impedance matching capacitor to provide an input impedance for the second single-ended voltage signal to match a package trace impedance corresponding to the first photo-detector.

21. The optical receiver of Claim 18 further comprising:

a second photo-detector to receive a second optical signal and to generate a second current signal;

a second transimpedance amplifier circuit to convert the second current signal to a differential clock signal;

said clock recovery circuit having said phase interpolator to generate the aligned clock signal for said first differential voltage signal from the differential clock signal.

22. The optical receiver of Claim 21 further comprising:

a delay locked loop to generate a plurality of clock phases from the differential clock signal; and

said phase interpolator to generate the aligned clock signal from the plurality of clock phases.

23. An optical signaling system comprising:

a laser driver having a bias control and a modulation control, said laser driver to receive a first digital voltage sequence and to generate a first current signal having a bias mode adjustable by said bias control and a modulation mode adjustable by said modulation control;

a laser to generate a first optical signal responsive to the first current signal of the laser driver;

a first photo-detector to receive a second optical signal and to generate a second

current signal;

a first transimpedance amplifier circuit to convert the second current signal to a first differential voltage signal;

a clock recovery circuit having a phase interpolator to generate an aligned clock signal for said first differential voltage signal; and

a sampler circuit to generate a second digital voltage sequence responsive at least in part to the aligned clock signal and the first differential voltage signal.

24. The optical signaling system of Claim 23 further comprising:

a tunable buffered level shifter to shift an input of the laser driver to a controlled voltage level responsive to a transition of said first digital voltage sequence.

25. The optical signaling system of Claim 23, said laser driver further comprising:

a CMOS modulation circuit having a pMOSFET, a first nMOSFET and a second nMOSFET, the CMOS modulation circuit to cause the first current signal in the modulation mode to flow between the laser, the first nMOSFET and the second nMOSFET responsive to the input of the laser driver being shifted to a first voltage level, and to causes the first current signal in the bias mode to flow between the laser and the bias control when another current flows through the pMOSFET responsive to the input of the laser driver being shifted to a second voltage level.

26. The optical signaling system of Claim 25 wherein an input gate of the third nMOSFET is to reduce an overshoot of the first current signal.

27. The optical signaling system of Claim 23 wherein the laser is a VCSEL diode.

28. The optical signaling system of Claim 23 wherein adjusting the modulation mode of the current signal is accomplished by setting one or more inputs of the modulation control.

29. The optical signaling system of Claim 23 wherein adjusting the bias mode of the current signal is accomplished by setting one or more inputs of the bias control.

30. The optical signaling system of Claim 23 wherein said first transimpedance amplifier circuit complimentary couples a first single-ended voltage signal corresponding to the first current signal with a second single-ended voltage signal to generated said first differential voltage signal, and resistively couples said first and second single-ended voltage signals to attenuate a common signal noise.

31. The optical signaling system of Claim 30, said first transimpedance amplifier further comprising:

a differential impedance matching capacitor to provide an input impedance for the second single-ended voltage signal to match a package trace impedance corresponding to the first photo-detector.

32. The optical signaling system of Claim 23 further comprising:

a second photo-detector to receive a third optical signal and to generate a third

current signal;

a second transimpedance amplifier circuit to convert the third current signal to a differential clock signal;

said clock recovery circuit having said phase interpolator to generate the aligned clock signal for said first differential voltage signal from the differential clock signal.

33. The optical signaling system of Claim 32 further comprising:

a delay locked loop to generate a plurality of clock phases from the differential clock signal; and

said phase interpolator to generate the aligned clock signal from the plurality of clock phases.